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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/754,972	01/05/2001	Aaron M. Schoenfeld	303.736US1	3930

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EXAMINER	
CAO, CHUN	
ART UNIT	**PAPER NUMBER**
2115	

DATE MAILED: 05/26/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/754,972	Applicant(s) SCHOENFELD ET AL.	
	Examiner Chun Cao	Art Unit 2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27,43-54,68 and 69* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-27,43-54,68 and 69* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 January 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 2.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-70 are presented for examination. Claims 28-42,55-67 and 70 are canceled by applicant in paper no. 4. Claims 1-27, 43-54, 68 and 69 are remained in the application.

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed. The current title is imprecise.

Drawings

3. Figure 1 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1, 2, 6, 7, 9 and 68-69 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nelson et al. (Nelson), US patent no. 5,414,381 and in view of Lee et al. (Lee), US patent no. 6,141,292.

As per claim 1, Nelson teaches a synchronous integrated circuit device having an output bus for outputting a plurality of output signals, comprising:

An output circuit [figs. 4, 9] including a plurality of output signal paths [abstract all, figs. 4, 9; col. 6, line 17] configured to output [168, fig. 9] the plurality of output signals synchronously [fig. 10; col. 14, line 15] with the system clock signal [fig. 10] by the delay clock signal [162, fig. 9]; and

Wherein at least one of the output signal paths includes a delay circuit [fig. 5; 42, fig. 9] and an output buffer [164, fig. 9; col. 11, line 66] coupled to the delay circuit [fig. 9], each delay circuit configured to provide a programmable delay [col. 14, lines 62-66] to the delayed clock signal [162, fig. 9] to generate a unique delayed clock signal [fig. 5] which is used for clocking an output signal [56, fig. 9] into the respective output buffer [164, fig. 9].

Nelson does not teach a synchronous integrated circuit device comprising:

a clock input buffer configured to receive a system clock signal and to generate a buffered clock signal; a delay line coupled to the clock input buffer, the delay line configured to receive the buffered clock signal and to generate a delayed clock signal.

Lee teaches a synchronous integrated circuit device comprising:

a clock input buffer [11, fig. 1; col. 3, line 56] coupled to the clock input buffer [fig. 1], the delay line configured to receive the buffered clock signal [fig. 1] and to generate a delayed clock signal [col. 3, lines 65-67].

It is obvious to one of ordinary skill in the art to combine Nelson and Lee's devices because Nelson's invention is motivated to provide means and method for precisely adjusting signal delay, specially adjusting a signal delay [col. 3, lines 52-56],

and Lee's invention further stabilize the input clock signal by providing a clock input buffer and a delay line.

As per claim 2, Nelson teaches that the programmable delay provided by each delay circuit is programmed to decrease output skew across the output signal [col. 14, lines 62-66].

As per claim 6, Nelson teaches that the programmable delay provided by each delay circuit is programmed statically [col. 14, lines 62-66].

As per claim 7, Nelson teaches that the programmable delay provided by each delay circuit is programmed based upon output skew during operation of the device [col. 14, line 62-66].

As per claim 9, Nelson teaches that the device has an initialization mode of operation wherein the output signals are toggled, and the programmable delay provided by each delay circuit is programmed during initialization operation [col. 14, lines 37-66].

As per claim 68 is contained the same limitations and perform the same function as claims 1-2, therefore the same rejection is applied.

As per claim 69 is contained the same limitations and perform the same function as claims 1-2, therefore the same rejection is applied.

6. Claims 3-5, 8,10-27, 43-54 and 68-69 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nelson et al. (Nelson), US patent no. 5,414,381 and Lee et al. (Lee), US patent no. 6,141,292 as applied to claim 1 above, and further in view of Schulz (Schulz) US patent no. 6,340,905.

As per claim 3, Schulz teach that the device of claim 1, wherein the clock input buffer provides a first delay [134, fig. 1]; Nelson teaches of each output signal path provides a second delay [22, fig. 4]; and Schultz also teaches that the delay line [see Skew Adjust blocks in fig. 2] provides a third delay based upon a delay model of the sum of the first delay and the second delay [fig. 2; col. 7 lines 8-14].

It is obvious to one of ordinary skill in the art to combine Nelson and Lee and Schulz because Nelson's invention is motivated to provide means and method for precisely adjusting signal delay, specially adjusting a signal delay [col. 3, lines 52-56], and Schulz's invention further stabilize the input clock signal by providing delay lines that automatically adjust clock skew using feedback mechanism.

As per claim 4, Schultz teaches that a phase detector to control the delay line based upon a phase difference between the buffered clock signal and a signal generated by applying a delay model to the delayed clock signal [col. 11, lines 41-53; col. 7, lines 8-14].

As per claim 5, Schultz teaches the programmable delay provided by each delay circuit is programmed dynamically [col. 2, line 36].

As per claim 8, Schultz teaches the programmable delay provided by each delay circuit is programmed based upon an output skew between a first output signal that was output from the respective output signal path and a second output signal [see the input lines of Skew Detect 2 block, on coming from Skew Adjust 2 and the other coming from Skew Adjust 3 in fig. 2].

7. As to claims 10-14 are contained the same limitations and perform the same function as claims 1-4 and 8, therefore the same rejection is applied.

As to claims 15-16, inherently, Lee discloses a digital DLL and an analog DLL [col. 1, lines 27-30, 38-45].

8. As to claims 17-25 are contained the same limitations and perform the same function as claims 1-9, therefore the same rejection is applied. Furthermore, Nelson discloses the output data paths each include a variable delay circuit [col. 3, lines 65-68; figs. 5, 9]; and each delay circuit configured to provide an independent variable delay [col. 6, lines 15-23].

As per claim 26, Nelson discloses that one of the output signal paths is the slowest output signal path, and the variable delay provided by each of the delay circuits is individually programmed based upon the slowest output signal path so as to align the plurality of output signals, thereby decreasing skew across the output signals [col. 14, lines 37-67].

As per claim 27, Nelson discloses that one of the output signal paths is defined as a reference output signal path, the delay circuit for the reference output signal path provides a midpoint delay, and the delay circuits for the remaining output signal paths provide less or more than the midpoint delay if the corresponding output signal path is slower or faster than the reference output signal path, respectively [col. 14, lines 37-67].

9. as to claims 43-54, Nelson and Lee and Schultz together teach the claimed system. Therefore, Nelson and Lee and Schultz together teach the claimed method of steps to carry out the system.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chun Cao at (703) 308-6106. The examiner can normally be reached on Monday-Friday from 7:30 am - 4:00 pm. If attempts to reach the examiner by phone are unsuccessful, the examiner's supervisor Thomas Lee can be reached at (703) 305-9717. The fax number for this Art Unit is following: Official (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 306-5631.

Chun Cao

May 24, 2004